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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/332,338	06/14/1999	GUILLERMO J. ROZAS	TRANS11	2806

7590 09/06/2002

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EXAMINER
NGUYEN, DUSTIN

ART UNIT	PAPER NUMBER
2156	

DATE MAILED: 09/06/2002 #3

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/332,338	ROZAS ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2156	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1 – 21 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Cmelik et al. (US Patent No 6031992).

4. As per claim 1, Cmelik teaches a method for causing scheduler software to produce code which executes rapidly including the steps of:

reordering a sequence of instructions to run as fast as possible (e.g. col 12, line 3-13) even though the reordered sequence may generate an exception (i.e. no dependency checking) (e.g. col 15, line 1-9),

raising an exception if the reordered sequence of instructions violates a scheduling constraint (e.g. col 13, line 62-66), and

determining steps to be taken for correctly executing each set of instructions about which an exception is raised (e.g. col 13, line 26-36 and line 50-53).

5. As per claim 2, Cmelik teaches the step of raising an exception if the reordered sequence of instructions violates a scheduling constraint includes a step of detecting exceptions caused by reordered instructions in the reordered sequence (e.g. col 12, line 42-45 and col 14, line 17-21).

6. As per claim 3, Cmelik teaches the step of detecting exceptions caused by reordered instructions in the reordered sequence includes:

remembering an instruction which has been placed out of order in the sequence (i.e. translation buffer) (e.g. col 12, line 13-30), and

checking instructions in the sequence with respect to which the remembered instruction has been reordered to determine if an incorrect result is produced by the sequence of instructions (e.g. col 12, line 39-41).

7. As per claim 4, Cmelik discloses the step of remembering an instruction which has been placed out of order in the sequence includes

storing a memory address accessed by the instruction (e.g. col 13, line 8-18), and

the step of checking instructions in the sequence with respect to which the remembered instruction has been reordered to determine if an incorrect result is produced by the sequence of instructions includes comparing the stored memory address with memory addresses accessed by instructions against which it is checked (e.g. col 23, line 40-53).

8. As per claim 5, Cmelik teaches the memory address of the data accessed by the instruction is stored in a protection register (e.g. col 14, line 21-24 and col 37, line 19-23).

9. As per claim 6, Cmelik discloses a further step of remembering where all remembered instructions are held (e.g. col 14, line 10-16).

10. As per claim 7, Cmelik discloses it is probable that the reordered sequence will generate an exception (e.g. col 21, line 62-col 22, line 11 and col 23, line 21-23).

11. As per claim 8, Cmelik teaches the step of raising an exception if the reordered sequence of instructions violates a scheduling constraint includes a step of detecting exceptions caused by reordered instructions in the reordered sequence (e.g. col 21, line 39-44).

12. As per claim 9, Cmelik discloses the step of detecting exceptions caused by reordered instructions in the reordered sequence includes

remembering an instruction which has been placed out of order in the sequence (e.g. col 16, line 38-42), and

checking instructions in the sequence with respect to which the remembered instruction has been reordered to determine if an incorrect result is produced by the sequence of instructions (e.g. col 12, line 39-41).

13. As per claim 10, Cmelik teaches the step of remembering an instruction which has been placed out of order in the sequence includes

storing a memory address accessed by the instruction (e.g. col 23, line 35-40), and

the step of checking instructions in the sequence with respect to which the remembered instruction has been reordered to determine if an incorrect result is produced by the sequence of instructions includes comparing the stored memory address with memory addresses accessed by instructions against which it is checked (e.g. col 23, line 41-46).

14. As per claim 11, Cmelik discloses the memory address accessed by the instruction is stored in a protection register (e.g. col 14, line 21-24 and col 37, line 19-23).

15. As per claim 12, Cmelik discloses a further step of remembering where all remembered instructions are held (e.g. col 23, line 46-53).

16. As per claims 13-17, they are rejected for similar reasons as stated above. Furthermore, Cmelik teaches the functions and elements above can be performed in a computer system.

17. As per claim 18, Cmelik teaches the means for storing indicators for the memory addresses accessed by identified instructions (i.e. working and target registers) (e.g. col 16, line 38-56).

18. As per claim 19, Cmelik teaches

means for storing indicators for the memory addresses accessed by identified instructions which exist during a sequence of instructions (i.e. working registers) (e.g. col 17, line 9-12), and

means for storing indicators for the addresses accessed by identified instructions which persist beyond a sequence of instructions (i.e. target registers) (e.g. col 12, line 67-col 13, line 8).

19. As per claim 20, Cmelik teaches

the means for storing indicators for the memory addresses accessed by identified instructions which exist during a sequence of instructions is a first register storing instructions of valid memory addresses accessed by identified instructions (i.e. head pointer) (e.g. Figure 5, item 51),

the means for storing indicators for the memory addresses accessed by identified instructions which persist a sequence of instructions is a second register storing indications of valid memory addresses accessed by identified instructions (i.e. gate pointer) (e.g. Figure 5, item 52), and

further including a third register for storing indicators for the memory addresses accessed by identified instructions (i.e. tail pointer) (e.g. Figure 5, item 53), and

means for transferring indications from the second register to the first and third registers when a sequence of instructions is executed without an exception (i.e. commit) (e.g. col 17, line 54-65), and

means for transferring indications from the third register to the first and second registers when an exception is generated during a sequence of instructions being executed (i.e. rollback) (e.g. col 18, line 8-19).

20. As per claim 21, Cmelik teaches the means for replicating memory data in an execution unit register (e.g. col 23, line 30-35).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (703) 305-5321. The examiner can normally be reached on Monday – Friday (8:00 – 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alvin Oberley can be reached on (703) 305-9716.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directly to the receptionist whose telephone number is (703) 305-3900.

Dustin Nguyen
DN
09/07/02

JOHN A. FOLLANSBEE
PRIMARY EXAMINER